The below description refers to image processor developed by Erik Liskay

Howto use VHDL image processor:

1. In file manager, create a directory, and copy the following files there: Cell.vhd, ImageProcessor.vhd, Testbench.vhd, house\_SaltPepper\_600x390.data and mageB.data. These can be found in directory ImageProcessor.
2. In Questa Sim, create a new project, choosing the directory from step 1 above as project location.
3. After creating new project, the “Add items to the Project” popup window appears. Click on “Add Existing File” and choose “Cell.vhd, ImageProcessor.vhd and testbench.vhd”. Select the “Reference from current location” radio button, do not select “Copy to project directory”.
4. Close the “Add items to the Project” popup window.
5. Right click on one of the VHDL files within the Questa Sim file list in the “Project” tab, and select “Compile all”. Since the order of compile matters, you might have to repeat in order for all files to compile without error.
6. In Questa bottom left command window, type “vsim Testbench” and enter, now messages that design is being optimized will scroll in command window.
7. In Questa bottom left command window type “run –all” and enter. Now the processed image files will be written to the project directory. The image processor also runs on Mentor graphics Modelsim Student Edition.
8. The current “testbench.vhd” is set to run a range of opcodes. The variable ‘number” is the starting opcode, currently the last opcode is 2A (hexadecimal) which translates to 42. If adding new opcodes, the range needs to be continuous, otherwise the current testbench.vhd script will fail. All the opcodes except hex 2A (binary 42) are documented in Liskay report. Opcode 2A is a median of medians.

Howto change image input files

1. Start with any image format compatible with Gimp ( <http://www.gimp.org> ). Create an image where the horizontal and vertical pixel count is an integer multiplier of 30, i.e. Width=330, Height=240. Assume for now the image file is “image.jpg”.
2. Open image.jpg in GIMP.
3. Select File -> Export
4. In the Export Image file dialog, click on the “+” with title “Select file type by extension”, and choose “Raw image data” as file type. The saved file is now in the format required by the VHDL image processor.

Howto view the output files

1. The output format is “Raw image file”, file can be opened in GIMP, the image will be unscrambled when the correct width and height pixel count is manually entered.
2. Using the suffix “data”, and associating with GIMP, will allow opening raw output files by doubleclicking in file manager.
3. It might be convenient to run Questa Sim image processor on computer lab workstation, outputting to n-drive, and open aoutput files from personal computer with n-drive mounted, as PSU workstations don’t have GIMP installed yet.

Notes on usage:

The current “testbench.vhd” is set to run a range of opcodes. The variable ‘number” is the starting opcode, currently the last opcode is 2A (hexadecimal) which translates to 42. If adding new opcodes, the range needs to be continuous, otherwise the current testbench.vhd script will fail.

Howto use VHDL image processor:

1. Create a directory, and copy the following files there: Cell.vhd, ImageProcessor.vhd, Testbench.vhd, House\_snow\_600x390.data and imageB.data. (From ImageProcessor directory).
2. In Questasim, create a new project, choosing the directory from step 1 above as project location.
3. Add the files “Cell.vhd, ImageProcessor.vhd and Testbench.vhd” to project. Do not select “move to project directory”.
4. Right click on one of the VHDL files within the Questa file list in the “Project” tab, and select “Compile all”. Since the order of compile matters, you might have to repeat in order for all files to compile without error.
5. In Questa bottom left command window, type “vsim Testbench” and enter, now messages that design is being optimized will scroll in command window.
6. In Questa bottom left command window type “run –all” and enter.
7. The output will be 43 different image files, each one corresponding to an opcode documented in the Liskay report, plus Output42.data, which is a median of medians of 3, from opcode 2A.